CLAIMS

What is claimed is:

1. A slicer circuit in a receiver comprising:

a threshold voltage circuit generating a plurality of differential threshold signals; and

a differential comparator, the differential comparator including a first differential amplifier and a second differential amplifier, the first and second differential amplifiers cross-coupled to output a differential output signal dependent on a difference between one of the differential threshold signals coupled to the first differential amplifier and a differential input signal coupled to the second differential amplifier.

2. The slicer circuit as claimed in Claim 1 further comprising:

a plurality of differential comparators.

3. The slicer circuit as claimed in Claim 1 wherein a non-inverting input of the first differential amplifier is coupled to a first transistor and an inverting input of the first differential amplifier is coupled to a second transistor, a non-inverting input of the second amplifier is coupled to a third transistor and an inverting input of the second differential amplifier is coupled to a fourth transistor, the first and second differential amplifiers being cross-coupled by coupling the collector of the first transistor to the collector of the third transistor and coupling the collector of the second transistor to the collector of the fourth transistor.

4. The slicer circuit as claimed in Claim 1 further comprising:

a first emitter follower coupled to the first differential amplifier; and

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a second emitter follower coupled to the second differential amplifier, the differential output coupled between the first emitter follower and the second emitter follower.

5. The slicer circuit as claimed in Claim 2 wherein the transistors are bi-polar and operate in a linear region.

6. The slicer circuit an claimed in Claim 1 wherein the differential input signal is 600 milli Volts peak to peak differentially and the differential threshold signals are 200 mili Volts, -200 milli Volts and 0 Volts.

7. The slicer circuit as claimed in Claim 2 wherein the number of differential comparators is three.

8. A method for recovering data encoded in a received signal comprising:

generating a plurality of differential threshold signals;

coupling one of the differential threshold signals to inputs of a first differential amplifier;

coupling a differential input signal to inputs of a second differential amplifier, the second differential amplifier cross-coupled to the first differential amplifier; and

outputting a differential output signal dependent on the difference between the differential threshold signal and the differential input signal.

9. The method as claimed in Claim 8 wherein the first and second differential amplifiers are cross-coupled by coupling the collector of a first transistor to the collector of a third transistor and the collector of a second transistor to the collector of a fourth transistor, coupling a non-inverting input of the first

differential amplifier to the first transistor and coupling an inverting input of the first differential amplifier to the second transistor and coupling non-inverting input of the second amplifier to the third transistor and coupling an inverting input of the second differential amplifier to the fourth transistor.

10. The method as claimed in Claim 8 further comprising:

coupling a first emitter follower to the first differential amplifier and a second emitter follower to the second differential amplifier, the differential output signal coupled between the first emitter follower and the second emitter follower.

11. The method as claimed in Claim 9 wherein the transistors are bi-polar and operate in a linear region.

12. The method as claimed in Claim 8 wherein the differential input signal is 600 milli Volts peak to peak differentially and the differential threshold signals are 200 mili Volts, -200 milli Volts and 0 Volts.

13. A slicer circuit comprising:

means for generating a plurality of differential threshold signals; and

means for outputting a differential output signal dependent on the difference between one of the differential threshold signals and a differential input signal by coupling the differential threshold signal to inputs of a first differential amplifier and coupling the differential input signal to inputs of a second differential amplifier, the second differential amplifier cross-coupled to the first differential amplifier.

14. The slicer circuit as claimed in Claim 13 wherein a non-inverting input of the first differential amplifier is coupled to a first transistor and an inverting input of the first differential amplifier is coupled to a second transistor, a non-inverting input of the second amplifier is coupled to a third transistor and an inverting input of the second differential amplifier is coupled to a fourth transistor, the first and second differential amplifiers cross-coupled by coupling the collector of the first transistor to the collector of the third transistor and the collector of the second transistor to the collector of the fourth transistor.

15. The slicer circuit as claimed in Claim 13 further comprising:

a first emitter follower coupled to the first differential amplifier and a second emitter follower coupled to the second differential amplifier, the differential output signal coupled between the first emitter follower and the second emitter follower.

16. The slicer circuit as claimed in Claim 15 wherein the transistors are bi-polar and operate in a linear region.

17. The slicer circuit as claimed in Claim 13 wherein the differential input signal is 600 milli Volts peak to peak differentially and the differential threshold signals are 200 milli Volts, -200 milli Volts and 0 Volts.

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